REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-65 are presently active; Claims 1, 21, 26, 28, 48, 53, 55, 61, and 62 have been presently amended. No new matter has been added.

In the outstanding Office Action, Claims 1-47 were rejected under 35 U.S.C. § 112, first paragraph, as based on a disclosure that was non-enabling.[1] Claim 44 was rejected under 35 U.S.C. § 101.[2] Claim 1 was provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,501. Claim 1 was provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,507. Claim 1 was provisionally rejected under the judicially created doctrine of obviousness-type double patenting over Claim 1 of U.S. Pat. Appl. No. 10/673,138. Claims 1-11, 13-14, 17-19, 21-27, 28-38, 40-41, 44-46, 48-54, 55-57, and 60-62 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman et al. (U.S. Pat. No. 6,802,045) in view of Jain et al. ("Mathematical Physical Engine: Parallel Processing for Modeling and Simulation of Physical Phenomena"). Claims 12, 15-16, 20, 39, 42-43, 47, and 58-59 were rejected under 35 U.S.C. § 103(a) as being anticipated by Sonderman et al. in view of Jain et al. and Chen (U.S. Pat. No. 5,719,796).

Applicant acknowledges with appreciation the courtesy of Examiner Saxena and Primary Examiner Ferris to interview this case on December 4, 2006 during which time the issues in the outstanding Office Action were discussed as summarized hereinafter.

[1] Applicant believes that this rejection should have listed Claims 1-65 as the rejected claims.
[2] Applicant believes that this rejection should have listed Claim 62 as the rejected claim.

Regarding the rejection on the merits:

As clarified, Claim 1 defines a method of facilitating a process performed by a semiconductor processing tool including:

> 1) inputting process data relating to an actual process being performed by the semiconductor processing tool,
> 2) inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool,
> 3) performing first principles simulation for the actual process being performed ***during performance of the actual process*** using the physical model to provide a virtual sensor measurement in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, and
> 4) using the virtual sensor measurement ***obtained during the performance of the actual process*** to facilitate the actual process being performed by the semiconductor processing tool.[3]

As discussed during the interview, the Office Action asserts that "Sondermam clearly disclose providing simulation results for an actual process being performed (Sonderman: Col. 9 Lines 46-51 States)." Yet, this section of Sonderman et al. specifically discloses that:

> The system 100 then optimizes the simulation (described above) ***to find more optimal process target*** (T_i) for each silicon wafer, S_i ***to be processed***. These target values are then used ***to generate new control inputs***, X_{Ti}, on the line 805 to control ***a subsequent process*** of a silicon wafer S_i. The ***new control inputs***, X_{Ti}, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like. [emphasis added]

Thus, this section of Sonderman et al. clearly discloses that the simulation is to find a more optimum process target for each silicon wafer ***to be processed***. The simulation results produce a new control input for the silicon wafer ***to be processed***. Thus, Applicant respectfully submits that Sonderman et al. teach performing first principles simulation for the actual process being performed before performance of the actual process, and not the claimed

[3] The enumerations have been added purely for the purpose of referencing these elements in the present discussion.

performing first principles simulation for the actual process being performed during performance of the actual process. Thus, Sonderman et al. do not disclose and indeed ***teach away*** from the present invention. For at least this reason, Applicant submits that the present invention patentably defines over Sonderman et al.[4]

Furthermore, these deficiencies in Sonderman et al. are not overcome by Jain et al. Specifically, Applicant respectfully points out that the teachings of Jain et al., when considered as a whole as required under M.P.E.P. § 2143.01 VI, show the teachings of Jain et al., to be that of a proposed and non-enabled tool. Jain et al. disclose at pages 372-373 that:

> We ***propose*** a wafer scale implementation of the MPE. The starting point would be a dedicated processing cell, optimized specifically for the PDE arithmetic and data routing. Because of the relative simplicity of the cell, it ***is expected*** that extremely large arrays (8x8 to 32x32) ***could be*** successfully processed on a single piece of silicon using Wafer Scale Integration techniques. In fact, we have already laid the foundation for the development of such a processing cell. Our Universal Multiply-Subtract-Add [11] ***could be*** adapted for this first cell design. Similarly, our nonlinear coprocessor cell [12]-[14] ***might be used*** in conjunction with the UMSA to provide advanced mathematical functions. As suggested in Fig. 2, there would be courtyards of processors, each with two interconnection networks and two memory banks. 2-D, 3-D, and 4-D problems could then be mapped for parallel computations. Since inter-processor delays are very small (say a few ns), extremely high speeds could be achieved. This, together with the high degree of parallelism, would result also in high throughout. We ***envision*** 100 to 1000 processors (on one wafer) forming a wafer scale MPE. At a clock frequency of 50 MHz, a single wafer could achieve up to 20 GFLOPs performance. With our nonlinear coprocessor added, each instruction could equate to multiple floating point operations. Furthermore, because of the extendible architecture, several wafers ***could be*** interconnected as shown in Fig. 5 to construct a "stacked" MPE wafer system (SMPE). Note that no vertical interconnects within the stack of wafers are expected. Tens to hundreds of GFLOPs performance in a volume the size of a desk-top computer [15] ***could*** thus be achieved. However, ***these predictions*** ignore the likely technical advances ***in the next five years***; a tenfold further increase in performance ***might be achievable***. [Emphasis Added]

[4] The other sections of Sonderman et al. cited in the Office Action with regard to a first principles simulation being performed for an actual process indicate that a simulation result is used to "emulate the operations of an actual process control environment" and that the "process control environment 180 can receive data from the manufacturing environment 170 and the simulation environment 210 and make appropriate changes to manufacturing control parameters to affect operations of the manufacturing environment 170." These disclosures do not indicate when the simulation is performed.

Thus, one of ordinary skill in the art of semiconductor processing would not be motivated to combine the speculative and non-enabled teachings of Jain et al. with that of Sonderman et al. Moreover, even if combined, the teachings of Jain et al. would not suggest that the first principles simulation for the actual process be performed during performance of the actual process.

Hence, for all these reasons, independent Claims 1, 28, 55, and 62 are believed to patentably define over the applied art.

Moreover, dependent Claim 21 has been amended to define using a network of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation recited in Claim 1, as shown for example in Applicant's Figure 3. While Sonderman et al disclose at col. 9, line 58, to col. 10, line 5, the implementation of Advanced Process Control (APC) on a factory wide basis, there is no disclosure or suggestion in Sonderman et al for using a network of interconnected resources inside a semiconductor device manufacturing facility to perform the first principles simulation, as presently defined in Claim 21. While Jain et al. disclose interconnected computational resources, the interconnected resources in Jain et al. are between geographically displaced sites. There is not disclosure or suggestion in Jain et al. for using a network of interconnected resources inside a semiconductor device manufacturing facility. Indeed, Jain et al.'s teaching of the use of geographically displaced sites teaches away from Claim 21.

Similar arguments apply with respect to dependent Claims 48 and 61.

Thus, for their dependence on independent claims and these further distinctions from the applied art, Applicant submits that dependent Claims 21, 48, and 61 patentably define over the art of record.

Regarding the rejection under 35 U.S.C. § 112, first paragraph:

Applicant submits that the exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct the first principle simulation model is disclosed by Applicant's specification by numbered paragraphs [0035] and [0036] which state that

> First principles physical model 106 is a model of the physical attributes of the tool and tool environment as well as the fundamental equations necessary to perform first principles simulation and provide a simulation result for facilitating a process performed by the semiconductor processing tool. Thus, the first principles physical model 106 depends to some extent on the type of semiconductor processing tool 102 analyzed as well as the process performed in the tool. For example, the physical model 106 may include a spatially resolved model of the physical geometry of the tool 102, which is different, for example, for a chemical vapor deposition (CVD) chamber and a diffusion furnace. Similarly, the first principles equations necessary to compute flow fields are quite different than those necessary to compute temperature fields. The physical model 106 may be a model as implemented in commercially available software, such as ANSYS, of ANSYS Inc., Southpointe, 275 Technology Drive Canonsburg, PA 15317, FLUENT, of Fluent Inc., 10 Cavendish Ct. Centerra Park, Lebanon, NH 03766, or CFD-ACE+, of CFD Research Corp., 215 Wynn Dr., Huntsville, AL 35805, to compute flow fields, electro-magnetic fields, temperature fields, chemistry, surface chemistry (i.e. etch surface chemistry or deposition surface chemistry). However, special purpose or custom models developed from first principles to resolve these and other details within the processing system may also be used.
>
> First principles simulation processor 108 is a processing device that applies data input from the data input device 104 to the first principles physical model 108 to execute a first principles simulation. Specifically, the first principles simulation processor 108 may use the data provided by the data input device 104 to set initial conditions and/or boundary conditions for the first principles physical model 106, which is then executed by the simulation module. First principles simulations in the present invention include, but are not limited to, simulations of electro-magnetic fields derived from Maxwell's equations, continuum simulations, for example, for mass, momentum, and energy transport derived from continuity, the Navier-Stokes equation and the First Law of Thermodynamics, as well as atomistic simulations derived from the Boltzmann equation, such as for example Monte Carlo simulations of rarefied gases (see Bird, G.A. 1994. Molecular gas dynamics and the direct simulation of gas flows, Clarendon Press). First principles simulation processor 108 may be implemented as a processor or workstation physically integrated with the semiconductor processing tool 102, or as a general purpose computer system such as the computer system 1401 of Figure 14. The output of the first principles simulation processor 108 is a simulation result that is used to facilitate a process performed by the semiconductor processing tool 102. For example, the simulation result may be used to facilitate process development,

process control and fault detection as well as to provide virtual sensor outputs that facilitate tool processes, as will be further described below.

Thus, support for "inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool" is clearly recognized by at least this section of the specification.

Hence, it is respectfully submitted that the 35 U.S.C. § 112, first paragraph, rejection should be withdrawn.

Regarding the rejection under 35 U.S.C. § 101:

Regarding Claim 62, M.P.E.P. § 2106 .01 I. (a) indicates in the second paragraph that a claimed computer-readable medium ***encoded with a computer program*** is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer's functionality to be realized and is thus statutory.

Thus, it is respectfully requested that the rejection to Claim 62 under 35 U.S.C. § 101 should be removed in view of the present amendments.

Regarding the provisional double-patenting rejection:

Applicants submit that a terminal disclaimer can be filed, if the claims in the present application and the claims in the co-pending Application No. 10/673,501; 10/673,507; and 10/673,138 remain obvious in view of each other at the time of allowance of either of these applications. Indeed, M.P.E.P. § 804.02 IV states that, prior to issuance, it is necessary to disclaim each one of the double patenting references applied. Hence, Applicants respectfully request that the examiner contact the undersigned should the present arguments be accepted

and should the case be otherwise in a condition for allowance. At that time, a terminal disclaimer can be supplied to expedite issuance of this case.

Outstanding Information Disclosure Statement

Lastly, Applicant requests **again** that the Information Disclosure Statement filed September 15, 2005 (a copy of which is available on the Patent Application Information Retrieval System at the U.S. Patent and Trademark Office) be considered and the accompanying PTO Form 1449 be initialed and returned.

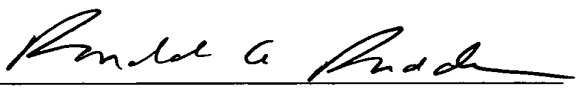
Conclusion:

As argued above, the outstanding rejections for this patent application should be removed, placing all the claims in a condition for allowance.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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